Workshop RENAFAE 2021: Projetos para o Futuro da Física de Altas Energias no Brasil

Read out electronics for the ALICE Forward Calorimeter (FoCal)

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for the Brazilian ALICE community

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Brazil in the ALICE experiment



Brazil in the ALICE experiment



Main physics motivation: Gluon PDF at small x







- Rise of gluon density natural for linear QCD evolution describing parton splitting
- Expected to be tamed by non-linear QCD evolution functions describing parton recombination, perhaps leading to saturation at the saturation scale Qs

Physics programme a forward calorimeter

• Quantify nuclear modification of the gluon density at small-x

Isolated photons in pp and pPb collisions

Explore non-linear QCD evolution

• Azimuthal $\pi^{0-}\pi^{0}$ and isolated photon π^{0} (or jet) correlations in pp and pPb collisions

Investigate the origin of long range flow-like correlations

 Azimuthal π⁰⁻h correlations using FoCal and central ALICE (and muon arm) in pp and pPb collisions

Explore jet quenching at forward rapidity

● Measure high p^T neutral pion production in PbPb

Other measurements

- Jets and dijets in pp/pPb and UPC
- Quarkonia in UPC (and pp*)
- Photon and pion HBT (*)
- W,Z in pp/pPb?
- Isolated photons in PbPb (*)
- Measurements at 14 TeV
 - Universality at small-x
 - Saturation in pp









 J/ψ photoproduction in ultra-peripheral p-Pb collisions



A possibility to investigate the gluon saturation by measuring J/ ψ in the forward region: FoCal will allow to detect J/ ψ decaying in lepton/antilepton.

Available experimental results already point to saturation effects, as well as not perturbative nature of QCD theory when x goes smaller ($x \rightarrow 10^{-6}$) Strong interest in experimental results for x<10⁻⁶ to better constrain nuclear PDF.

Expected performance an impact on nPDF

-ALICE projection

FoCal upgrade

p-Pb $\sqrt{s_{NN}} = 8.8 \text{ TeV}$

5

 $H_{\rm pPb}$

1.5

0.5

ᅇ



R. Khalek et al., arXiv:1904.00018

nNNPDF 1.0

²⁰⁸Pb reweighting

EIC fit

10⁻²

10⁻¹

FOCAL fit Q²=10 GeV² 90% CL

 Significant improvement (up to factor 2) on EPPS16 gluon PDF

10

Isolated γ

EPPS16+CT14

nNNPDF1.0

 $4.25 < \eta_{\rm cms} < 4.75$

15

20

p_ (GeV/*c*)

 $L = 50 \text{ nb}^{-1}$

- Similar improvement as from open charm
 - Test factorization/universality
- Below 4 GeV: challenging regime
 - Also measure direct photons by statistical subtraction

Recent nuclear PDFs: nNNPDF from DIS and minimal theoretical assumptions

 10^{-3}

• No constraints for x < 10⁻² from DIS

 10^{-4}

10⁻⁵

10-6

Б

- FOCAL provides significant constraints over a broad range: ~10⁻⁵ - 10⁻²
- Outperforming the EIC for x < 10⁻³



 Below ~6 GeV, uncertainty rises due to remaining background х

FoCal Proposal

FoCal-E: high-granularity Si-W sampling calorimeter for photons and π^0

FoCal-H: conventional metal-scintillator sampling calorimeter for photon isolation and jets

Observables:

- π^0 (and other neutral mesons)
- Isolated (direct) photons
- Jets (and di-jets)
- + J/ ψ (Y) in UPC
- W, Z
- Event plane and centrality



FoCal-E conceptual design



LG layer

HG layer

Final layout optimization ongoing for TDR:

- Location of pixel layers
- Number of pad layers
- Sensitive area at front for CPV/eID

absorber

• Conflicts with other detectors and services.

• Main challenge: Separate γ/π^0 at high energy

- Two photon separation from π^0 decay (p_T=10 GeV, η =4.5) ~5mm
- Requires small Molière radius and high granularity readout
- Si-W calorimeter with effective granularity $\approx 1 mm^2$

Studied in simulations 20 layers: W(3.5 mm \approx 1X₀) + silicon sensors

Two types: Pads (LG) and Pixels (HG)

- Pad layers provide shower profile and total energy
- Pixel layers (ALPIDE) provide position resolution to resolve overlapping showers



12/7/21

FoCal-H conceptual design



12/7/21

• No longitudinal readout required

1.1 m long: ~6 λ Tower size: 2-5 cm ~1k towers 880

PAD module design

Read-out ASIC: HGCROC (CMS HGCAL)

- 72 channels per chip: ADC + TOT
- Dynamic range: MIP to 2 fC
- Internal buffer; data shipped on readout

PCB carries 5 sensors (72 pads each), 5 HGCROC: ~50x8.3 cm



HGCROC tests and board design ongoing: LPSC, Grenoble

sub-module: PCB+Sensors+W plate



Experience with module assembly and design at Tsukuba Univ., Tsukuba Tech



KCU105

We are collaborating with the LPSC group in the test and qualifying of the board and HGCROC chip

ASIC designed by OMEGA-IN2P3 for HGCAL in CMS

- 72 channels + 4 channels for common mode subtraction + 2 special calibration channels
- 32b Digital Data continuously stored in 512 length DRAM @40MHz
- 72 ch. x 32b x 40MHz: huge data volume
- → Only Local-L1-triggered data are read out
- Idle packet is continuously sent out when no L1-trigger is activated
- The data processing for the trigger "information" path
- 32b: 4b header + 7b x 4
- Sum of 4 or 9 channels depending on the sensor



IFUSP and UFRGS have experience in readout electronics and test/validation of detectors, ASICs, and FECs.

- Test stations are going to be mounted at IFUSP (and at UFRGS too, at least a set up for developing protocols and code for test procedures) aiming:
 - "Independent" test and validation of the PAD-readout front-end board
 - Possibility to test the electronics (both the HGCROC and the complete board) against harsh conditions (mainly temperature and radiation)
 - Long term stability and aging tests
 - Qualifying the HGCROC before mounting it on the board

FoCal status: test beam in September

- Pad sensor geometry being optimized
 pad location for better coupling with the electronics
- Starting analysing the finest details of integration (e.g. cables "invading", narrowing, the corridor to go inside the L3 magnet, to the inner detectors)
- Prototyping the front-end boards, as well as interface boards to DAQ
- Possibility to generate a trigger still under study
- Pandemic introduced, it is still introducing, several delays for all labs (a bit more for us in Brazil)
- A test beam is presently scheduled for late September:
 - Testing in real conditions the "unitary" board (1 sensor, 72 pads), as well as interface to DAQ
 - Testing integration PAD-Pixels
 - Studying the performance of the 18 (LG) + 2 (HG) stack, and the effects of the gaps due to the electronic boards



Summary

Project	Alice FoCal (Read-out electronics for the Si-Pads detector)
Institutions	Brazil: IF/USP; IFGW/UniCamp; UFABC; IF-UFRGS. main international collaborators: LPSC (Fr); Tsukuba (Jp).
Timeline	 2021: R&D (prototyping FECs, testbeam, etc.) 2022: TDR 2023: finalizing & freezing the design 2024-2026: construction and test of modules 2025-???: pre-assembling and calibration; Installation and commissioning
Cost and funding	contribute to the construction of the low granularity (Si-PADs) readout: ≈150 kCHF, submitted to FAPESP (as part of a wider 'tematico' project presently under evaluation)
possible synergies	sharing experience in testing and validating ASIC and read-out electronics. Development of dedicated boards/circuits for dedicated tests. Sharing experience on FPGAs use.
possible spin-off	Yes, generic. In the context of development of ASIC and Readout systems (electronics for local application; build up experience and partnership for future activities)

Backup slides

FoCal vs LHCb: sensitivity to nPDF

LHCb-FIGURE-2020-006





- LHCb analysis approach: identify signal by BDT based on a combination of variables, e.g. isolation energy
- Improvement in S/B significantly smaller than of FoCal
- Leads to factor 2 or larger systematic uncertainty compared to FoCal
 - Expected performance depends on uncertainty on remaining background

(WP at ε_{sig} =0.2 for LHCb, at ε_{sig} ~0.4 for FoCal)

FoCal vs LHCb: sensitivity to nPDF



FoCal uncertainties

LHCb projected uncertainties (5% vs 10% uncertainty on the background)

Significantly better performance on nuclear PDF expected by FoCal measurement (in addition one unit higher reach in pseudorapidity, i.e. factor 3 smaller x reachable)

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Data rate estimate: pp@1Mhz

Data rate estimation for each pad layer





Possible to share GBT-FPGA to several pad layers

- → Design for the maximum rate
 - → @3.2Gb/s with FEC (8ob @4oMHz)
 - → @4.8Gb/s w/o FEC (112b @40MHz)
- → Reduce the number of needed GBT-FPGA
- → Reduce the number of needed CRU